HANDBOOK

for

RAPCO 104 SERIAL CODE READER

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W A R N I N G

PRECAUTIONS MUST BE TAKEN TO ENSURE THAT BOLTS BEING SCREWED INTO THE SIDE RAILS DO NOT PROTRUDE INSIDE THE CASE OTHERWISE DAMAGE TO COMPONENTS MAY RESULT.

SIDE RAIL THICKNESS = $\frac{1}{4}$"

RAPCO 104 SERIAL TIME CODE READER

The 104 Serial Code Reader will accept as its input either XR3 (250Hz carrier) or 2137 (1kHz carrier) in either the forward or reverse direction.

It will decode the serial code and then display the result.

The intensity of the LED display may be adjusted by front panel controls.

The Serial Code Reader has a 1-$\frac{3}{4}$" panel height and is 8-1/8" wide.

SPECIFICATION

INPUT

Code Format	:	XR3 or 2137, selected by rear panel switch.
Data Transmission Method	:	Amplitude Modulated Carrier
Carrier Frequencies	:	XR3 - 250Hz 2137 - 1kHz
Modulation Ratio	:	6:1 to 2:1
Amplitude	:	50mV to 25V
Input Impedance	:	100kΩ
Max. Safe Input	:	± 100V
Frequency Range	:	30 - 300kHz
Code Direction Sensing	:	Automatic

FRONT PANEL INDICATORS

Code Direction	:	Code Forward Code Reverse
Input Low	:	Will illuminate when input signal falls below a preset level.

A.C. POWER UNIT

Voltage	:	120V a.c. or 240V a.c. Selection via recessed switch on rear panel.
Input Frequency	:	47 - 400Hz
Power	:	15VA max.
Protection	:	0.5A 20mm Fuse

DISPLAY

(1) Six digit, seven segment, 0.43" high LED display with facility to alter brightness.

(2) Facility to test display.

MECHANICAL

The unit is 8-1/8" wide x 1-3/4" high x 9-1/2" deep.
Four configurations are available:

(1) Free standing. The two sides each have two tapped OBA holes enabling the instrument to be mounted by brackets to existing racking equipment.

(2) A table top stand is available. The stand incorporates pre-set friction pivots which enable the instrument to be adjusted for viewing angle from 30° below to 75° above the horizontal.

(3) Two units may be mounted side by side in a standard 19" rack. There is sufficient clearance for two units to be mounted in a tray which can itself be mounted on runners and still occupy only 1U (1-3/4") height.

(4) A single unit may be mounted centrally in a 19" rack. A rack mounting kit is available comprising brackets and front panel extension pieces.

WEIGHT

Free standing	:	1.5kg approx.
With Table Top Stand	:	2.2kg approx.

TEMPERATURE RANGE

Operating	:	0°C to +60°C
Storage	:	-20°C to +85°C

INSTALLATION

(1) Refer to the input specifications for the correct input operating conditions.

(2) Connect the serial time code to one of the rear BNC connectors.

(3) Select the correct carrier frequency i.e. 1kHz for 2137 or 250Hz for XR3.

(4) IMPORTANT - check that the mains voltage selector is at the correct setting.

(5) Press the power switch on the front panel to 'ON'

(6) Adjust the display intensity to the required level.

Display Intensity Setting

It is possible that the display will not illuminate when the mains power is applied. This is probably due to an illegal BCD number in the internal counter chain. A quick check for power is to depress DISPLAY TEST, the displays will then show all 8's. Depressing the INC button should then bring the display intensity up gradually. When switching on, an input signal should be applied as the logic will then clear any illegal BCD characters from the counter chain which would otherwise blank the display. The indicators for INPUT LOW and CODE DIRECTION are controlled by the intensity setting but will not be affected by these illegal characters.

Setting the Mark Threshold

This adjustment should be carried out with the aid of a dual trace oscilloscope.

One trace of the oscilloscope should monitor the normalised output on the AGC amplifier card (Test Point A), the second trace should monitor Test Point C on the same card. OV may be obtained either from the BNC connectors at the rear of the unit or Test Point G on the card. The oscilloscope traces should be zeroed to the same level and set to the same Y-axis setting.

Apply the input signal to the 104, preferably from the source from which this unit will normally be reading. Adjust the preset resistor until the lowest amplitude peak ('mark') of the large cycles still crosses the DC level trace. The more positive the level, the greater the range of modulation index that the 104 will accept. However, the unit will be less tolerant of poor signals.

If the source is normally a tape deck where it is unlikely that the modulation index will be changed then the ideal setting will be when all the 'mark' pulses extend more positive than the DC threshold whilst the carrier itself does not reach this level.

CIRCUIT DESCRIPTIONS

The 104 consists of four printed circuit boards - a Mother board, a Display board, a Decoder board and a board for the AGC amplifier. There is a position on the mother board for another daughter board bringing out parallel time information in 1 2 4 8 BCD form.

Mother Board

This board contains all the power supply components with the exception of the circuit breaker. The logic for the display brightness facility, a counter chain, shift registers and display driving components are all mounted on the mother board.

N1, 2, 3, 4, 5 form a 20 bit shift register. The data, clock and direction signals originate on the Decoder board and are coupled by pins 13, 12 and 16 respectively. The data is shifted in serial form. When the decoder recognises the reference mark it outputs a logic signal to Pin 6. C9 and R5 differentiate this signal on its negative going edge. N14 squares this and counter chain N8, 9, 10, 11, 12 and 13 update their contents to the existing value contained within the 20 bit shift register. It should be remembered that at this point the decoded value was almost one second 'slow' as the code transmitted comes after the reference time point. When the logic signal at pin 6 returns to logic 1, C8 and R4 differentiate it and N14 squares it. If the code direction is forward, the output from N14 (Pin 12) will update the counter chain by 1 thus anticipating the next reference time value. In the reverse direction, the coded value is effectively ahead of the reference mark and therefore no 'anticipation' is required. The counter chain is prevented from adding one second by pin 5 of N13 being held at logic 1.

The latches contained within the display decoder/drivers N15, 16, 17, 18, 19 and 20 normally 'follow' the contents of the counter chain.

However, when the 'INPUT LOW' lamp illuminates, these latches are frozen.

The variable display brightness function is performed by N.22, 23, 24 and 25. A gate within N14 is used as an oscillator, its running frequency of 100kHz is determined by R3 and C7. N22 is a binary counter that is continually counting on the output from the 100kHz oscillator. N25 is another oscillator running at approximately 2Hz. Its output is differentiated by C12 and R7. When a different level of display intensity is required either the 'INC' or 'DEC' pushbutton will be depressed. Pressing either of these buttons puts a logic 0 on the C_{In} terminal of the Up/Down binary counter N24. However, 'DEC' also changes the direction of counting from up to down by putting a Logic 0 on pin 10. N24 then starts to count at a 2Hz rate. When the counter becomes full (count of 15) or empty (count of zero) dependent upon count direction, C_{Out} pin 7 changes to a Logic 0 and prevents the clock pulses from passing through N.6

The four-line outputs from N22 and N24 are compared by N23. The A>B output from N23 is then used to modulate the displays via the blanking inputs on the display decoder chain. This system of controlling the intensity gives a constant frequency, variable (depending upon the value set in N24) mark to space ratio. Generally, the 7-segment displays are checked for minimum segment intensity variation at their specified working current i.e. in the range 10 - 20mA. To reduce the current linearly below this value will result in uneven, and in extreme cases, unacceptable segment intensity variation. This digital method of altering intensity overcomes this inherent disadvantage of LED displays.

The power supply is quite standard. A toroidal transformer is used for size considerations. Two three-pin regulators are employed in this unit. An extra low power 5V has been incorporated to enable external equipment to be powered from the 104 when the BCD option has been incorporated.

AGC Amplifier and Comparators (Refer to Drg. 104-1270)

This daughter board is the interface between the incoming signal and the digital system. The incoming signal is normalised to approximately 1V p-p at the output of the amplifier. Comparators are then used to extract the carrier information (frequency) and the 'marks' information.

The incoming signal is passed via C1 to R1. This removes any DC level present. The main amplifier is IC.1. The maximum gain is approximately 43 determined by R1, R2 and R3.

Components IC2, R4 and C4 form an integrator which extracts the DC content from the output of IC.1 due to the voltage offset of the amplifier and applies a corrective voltage to its positive input. The second amplifier in IC2 inverts the output from IC.1. A link will then select either the inverted or normal code to the following circuit. This feature is included because when reading code from the direct channel of tape recorders it will be found that the positive and negative modulation envelopes differ. One half will be approximately square reproducing the waveform recorded whilst the other half appears to have passed through a filter such that the square edges of the envelope have become rounded. This will lead to reading errors if the

stripping circuits have been arranged to work from this half. Generally it has been noted that the positive half of the envelope from direct recordings is square and it is the lower half that suffers from this distortion.

The output from the link is compared with a reference value of approximately 500mV derived in a resistor chain R15, VR1 and R14 by a comparator contained within IC3. The output from this comparator is used to modify the voltage stored across C6. This voltage is used to control the gate of FET T1 which in turn controls the input level to the main amplifier. The output from the link is also connected to two comparators. One comparator is connected as a Schmitt trigger together with R10 and R13 and compares the output with 0V giving a squared up carrier output. The second comparator detects the 'marks'.

The DC threshold level is set up by VR.1. R16, R17 and R20, R21, MR6 are used as level translators for the following digital circuitry. The low input signal indication is generated by comparing the input signal with a voltage derived by resistor chain R18, R19. The comparator output modifies the voltage across C10. In the absence of any input signal, the voltage across C10 will rise at a rate determined by R3 until transistor T2 switches on. T2 is used to drive the front panel indicator, to freeze the display and, when the BCD Buffer option is fitted, is brought out on the rear connector as SIGNAL LOW.

The Decoder

This board uses a counting technique to decode the incoming serial information. In addition, the direction of the code is also derived and used to switch the shifting direction of the register chain on the mother board.

The two signals coming from the AGC Amplifier board are processed by what is essentially a dual input edge triggered flip-flop N21 on the mother board. The advantage of this method is to transfer the noise immunity of the Schmitt trigger that produces the carrier output to the 'mark' signal that does not have this immunity.

The counter chain section 1 N9 and section 1 N7 count the mark pulses. N8 is used to switch the carrier frequency. In this text a 1kHz carrier will be assumed, important parameters for 250Hz will be noted in parentheses.

The second section of N4 is configured as a D-type flip-flop and determines when the 'marks' have stopped. It is reset by the positive edges from pins 9 and 10 of N8. This will give some immunity from noise spikes on the input as a minimum of 4 (1) mark pulses are required to reset N4. Thereafter N4 is clocked on the output pin 11 of N5.

This gate allows the carrier through when the marks have finished. When pin 11 of N4 goes to Logic 1 this is inverted by N3 and used to inhibit N4. This signal is inverted once again by N3 and is used to trigger flip-flop N2. Pin 13 of N2 is delayed by R1, C2 and then squared by N3, input pin 9. The output from N2 pin 13 also clocks the logic level present at pin 5 N1 into the flip-flop. At the same time, the output of N3 pin 8 is inverted, after passing via resistor R2, by N4 input pin 4, and used to reset the counter chain of N9, N7 and flip-flop N2 reset pin 10.

This logic level present at pin 5 N1 at the time it is entered into the latch is the data that will be clocked into the shift registers. However, if the total number of 'mark' pulses is less than 8 (2) or more than 32 (8) as determined by logic gate N5 input pins 5 & 6, then the shift register clock is inhibited.

This decoder recognises 8 (2) to 15 (3) 'mark' pulses as corresponding to Logic 0, and 16 (4) to 31 (7) as Logic 1. This will give some immunity against spurious 'marks'. Pin 13 of N7 will go to Logic 1 after 32 (8) 'mark' pulses. This is recognised as the reference mark in the code. Thus a Logic 1 will be present on pin 5 N2. When the 'marks' stop, N2 is released from its reset mode and will clock the logic state as pin 5 into the latch. The complementary output is brought out to pin 6. The action of this signal is explained in the section describing the Mother board.

Direction sensing is carried out by the second section of N9, N7 and N6. Again the counting is modified by N8 depending upon the carrier selection. For the sake of this description, a carrier of 1kHz will be assumed, figures for 250Hz will be shown in parentheses.

The second section of N6 is reset by a Logic 1 at pin 1 of N2 which occurs when the reference mark is detected. It is triggered when the two counter sections N9 and N7 which have been counting up on the carrier reach a value of 32 (8) at which point they will latch up due to the feedback connection to pin 9 N9. These counters will be reset when the reference mark is again detected. When pin 13 of N6 changes to a Logic 1, the first section of flip-flop N6 will clock into its latch the logic state present on its D input. This logic state is determined by the second section of N4 which detects when the marks have stopped. If its Q_A output, pin 11, is at a Logic 1, this indicates that data has not been present in order to have reset this section. This will occur when the code is reversed, when there is a long period after the reference mark and when there are no 'mark' pulses. The output from this flip-flop N6 is used to set the shifting direction of the registers on the Mother board and activate the appropriate front panel code direction LED.

BCD BUFFER BOARD

This board accepts the BCD lines from the counter chain ICs 8 - 13 on the Mother Board and outputs TTL compatible three-state signals on a 25-way Cannon socket at the rear of the unit.

The input signals go via input protection resistors R1 to R24 to the three-state buffers IC1 - IC4. These ICs operate from a supply rail of 5V in order that the output signals are TTL compatible. The outputs are put into a high impedance state by applying a logic 1 to Pin 25.

Specification:

OUTPUT: Three-state

DRIVE CAPABILITY: 1 standard TTL load

MAX. INPUT LEVEL AT HIGH IMPEDANCE CONTROL: +5.5V

PIN CONNECTIONS FOR BCD BUFFER OUTPUT - CANNON DB25S SOCKET (mating part supplied)

Pin No.	Function	
1	8	Seconds
2	4	
3	2	
4	1	
5	4	10's seconds
6	2	
7	1	
8	8	Minutes
9	4	
10	2	
11	1	
12	0V	
13	Forward/Reverse Signal (Forward = Logic '1')	
14	4	10's minutes
15	2	
16	1	
17	8	Hours
18	4	
19	2	
20	1	
21	2	10's hours
22	1	
23	$\overline{\text{Signal Low}}$ (Signal Low = Logic '0')	
24	+5V	
25	Hi Impedance or Carrier Select Input (internal link)	

Note For External Carrier Select operation, the manual carrier switch must be set to the 1kHz position then:
Logic 1 at input = 250Hz carrier
Logic 0 at input = 1kHz carrier

SECONDS MINUTES HOURS

DISPLAY

INC DEC TEST

INPUT LOW

DISPLAY H-P 5082-7653

DISPLAY 104-1241

N24 4516

N25 555

N23 74C85

4520

N14

TR1 2N3053

LAMP SUPPLY

4511 N20 4511 N19 4511 N18 4511 N17 4511 N16 4511 N15

PIN No's FOR OPTIONAL B.C.D OUTPUT BOARD

4510 N13 4510 N12 4510 N11 4510 N10 4510 N9 4510 N8

MR2 1N4148

AGC AMPLIFIER + STRIPPING CIRCUITS

2 x BNC SERIAL CODE IN

SEE DRG No. 759-1270

CARRIER MARK

N21

DECODER

SEE DRG No. 751-1272 (XR3/2137)

DATA CLOCK DATA DIRECT

1KHz 250Hz

CODE REVERSE R60 820

CODE FORWARD R59 82C

TR2 MPS A12 TR3 MPS A12

4194 N5 4194 N4 4194 N3 4194 N2 4194 N1

LINKING SHOWN FOR XR3/2137 CODES

R64 2K2

LINE 1 NEUTRAL 2 EARTH 3

FUSE

BRN RED BLK YELL. ORANGE VIOLET GREY BLUE 120↔240

REG 1 7812 REG 2 7812 REG 3 78L05

+12v TO DISPLAY + LOGIC

+12v TO ANALOGUE + DECODER LOGIC

R62 10K TR4 BC182L R63 10K

INPUTS FROM MOTHER BOARD

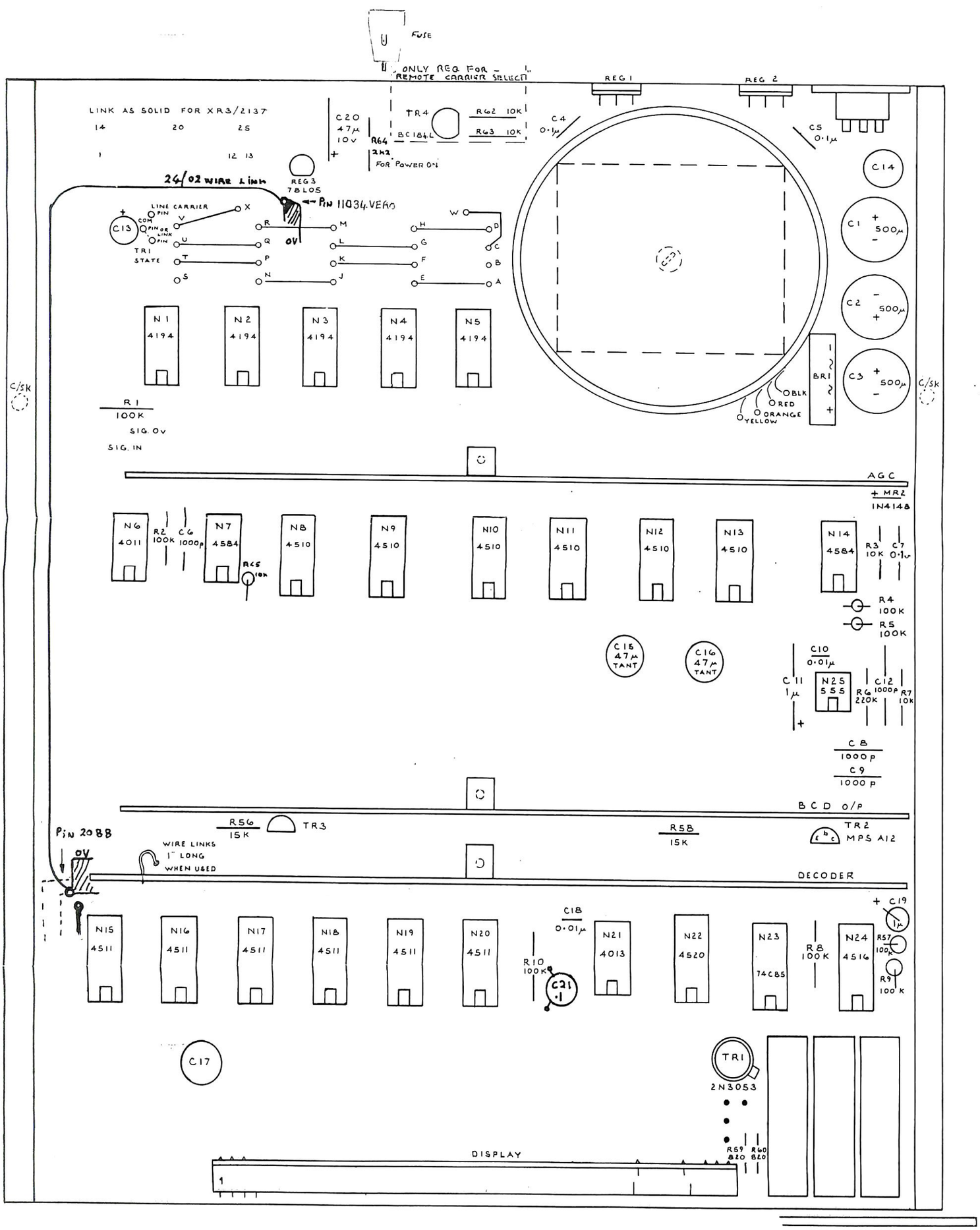
B.C.D. BUFFER 104-1244-1

SEC^S 10 SEC^S MIN 10 MIN HR^S 10 HR^S

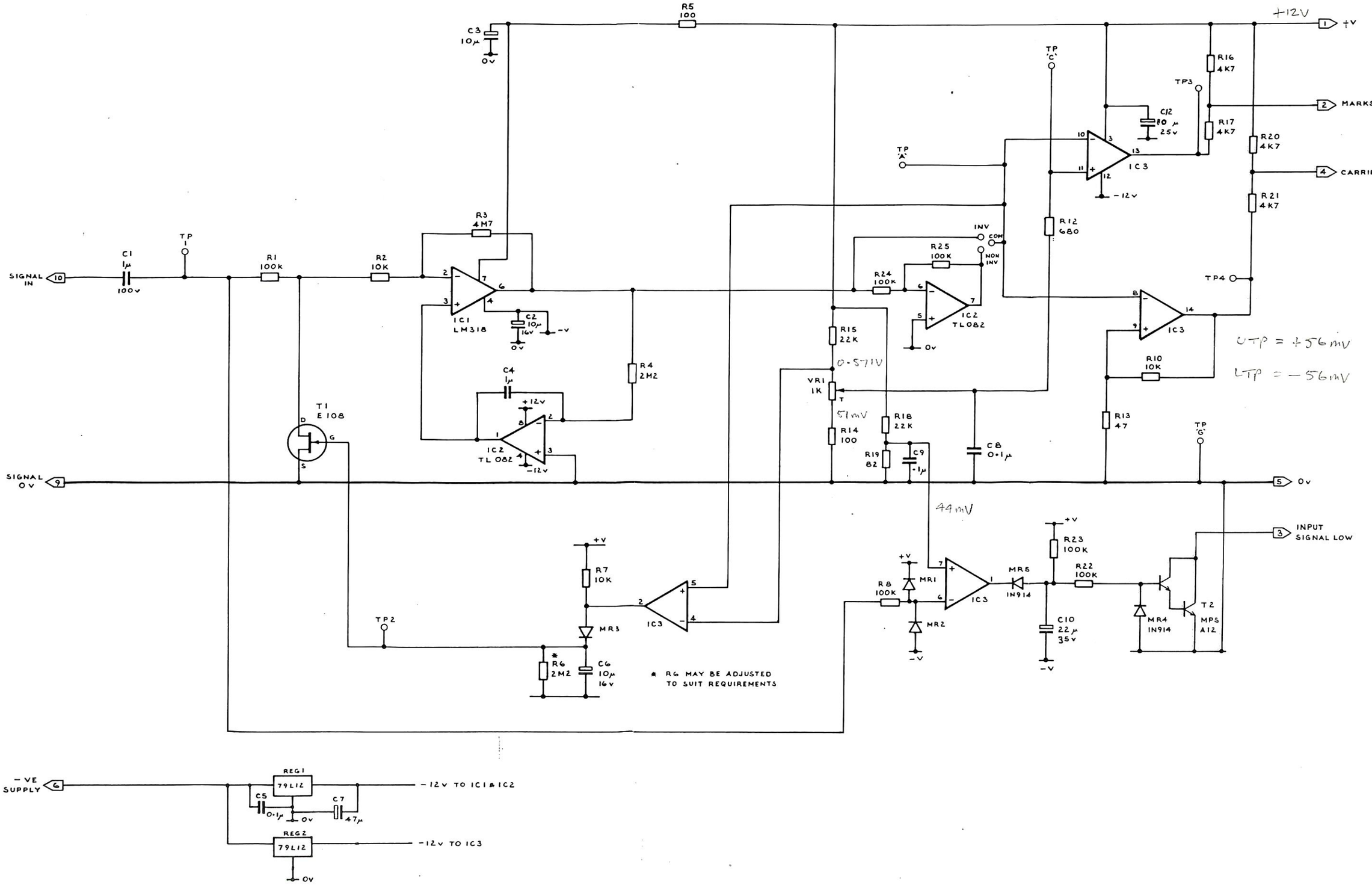
CANNON SKT. 'BCD OUTPUT'

TRI-STATE LINE CARRIER

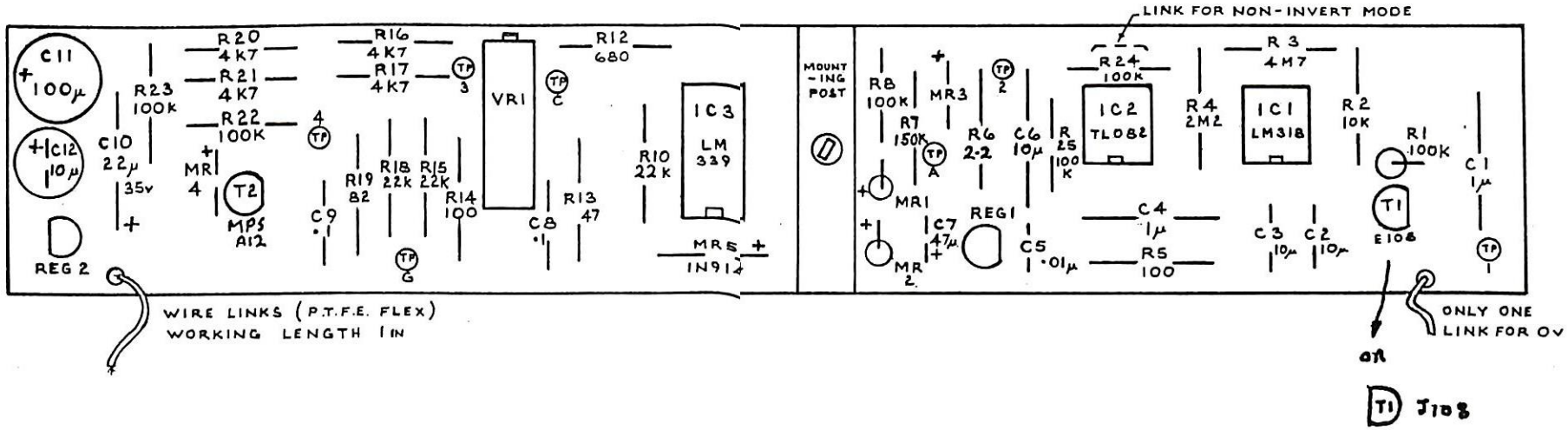
MOTHER BOARD 751-1240-4



MOTHER P.C.B
104-1240-4

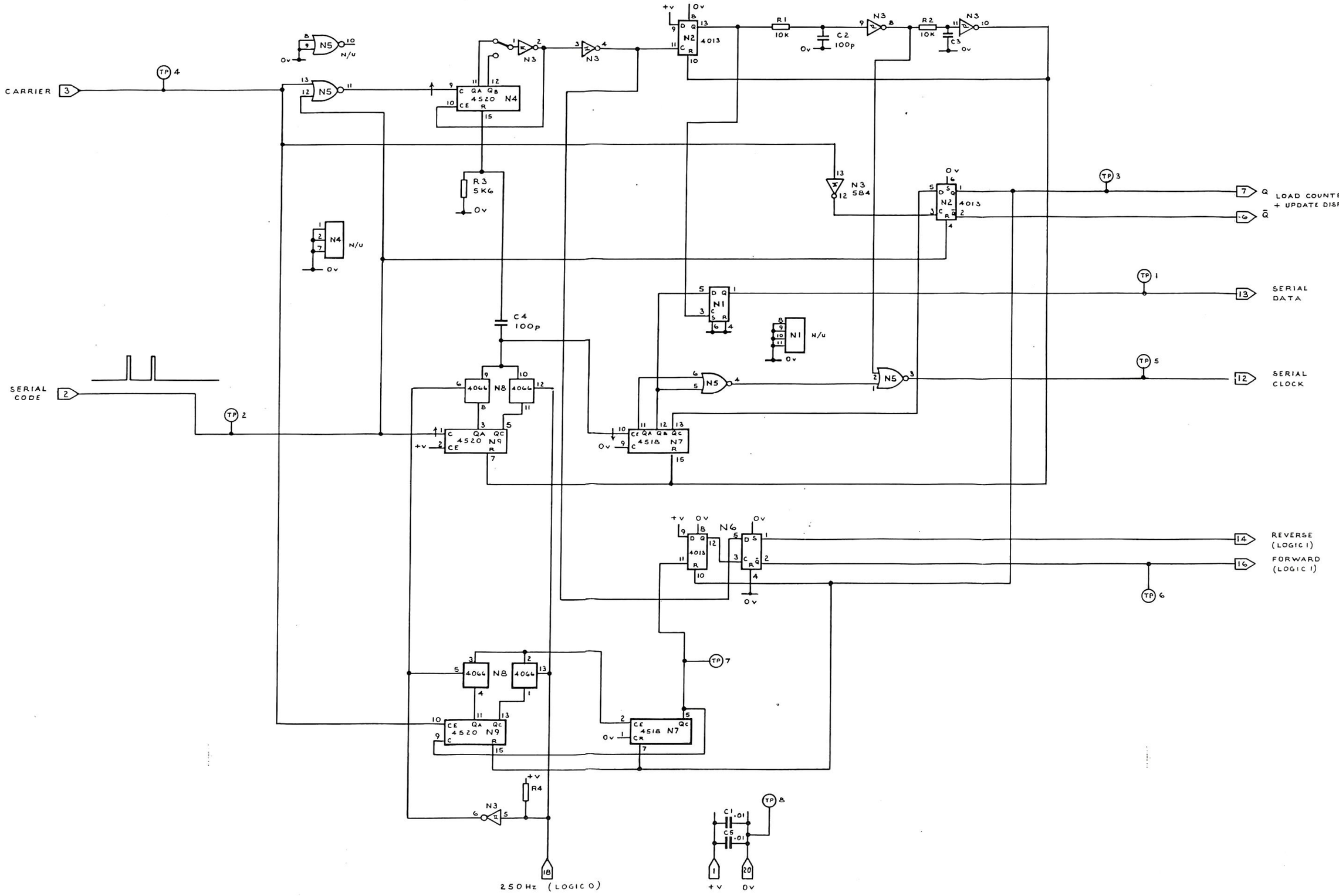


AGC AMP 104-1270-3



AGC AMP COMPARATORS

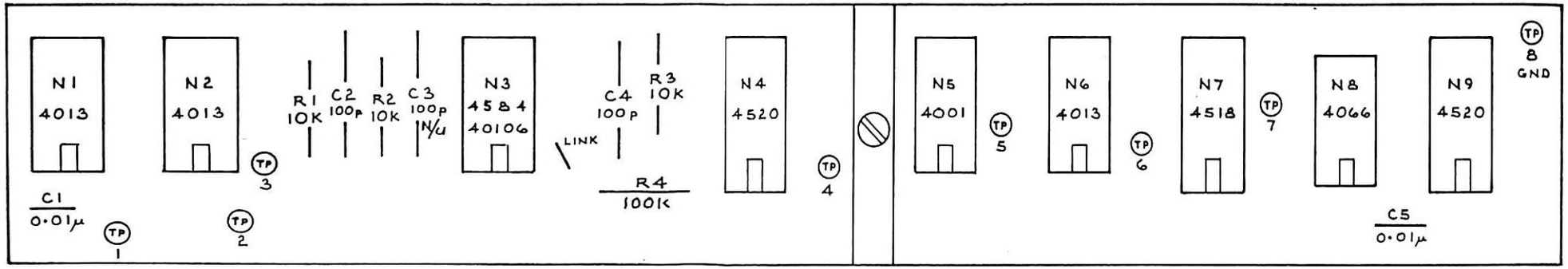
104-1243-5



DECODER XR3/2137

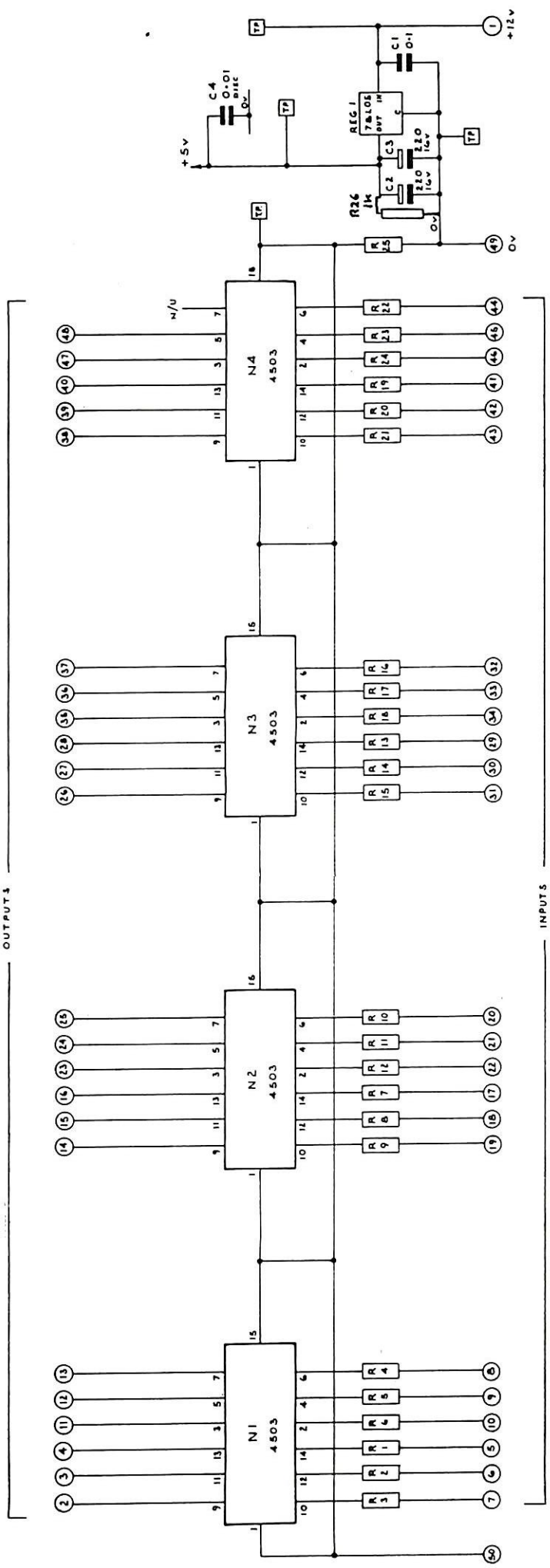
751-1272-1

XR3/2137 DECODER 751-1272-3

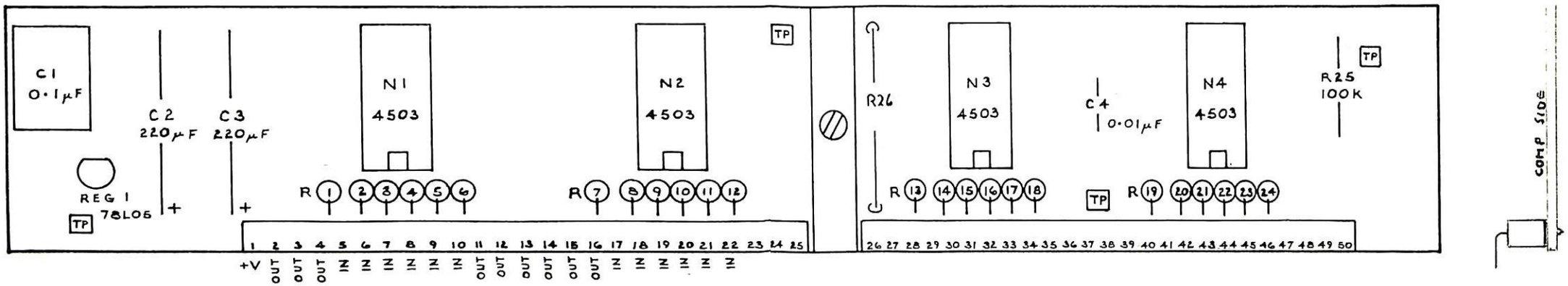


TEST POINTS

1. SERIAL DATA OUT (TO SHIFT REGISTER)
2. SERIAL CODE IN (MARKS)
3. UPDATE COUNTERS ETC. (DERIVED FROM REFERENCE MARK)
4. CARRIER INPUT (SQUARE WAVE)
5. DATA CLOCK (TO SHIFT REGISTER)
6. DATA DIRECTION (LOGIC 1 = FORWARD)
7. DIRECTION DETERMINING CIRCUIT UPDATE
8. 0 v



BCD BUFFERS 104-1244-4



BCD BUFFERS 104-1244-1